FIG. 1

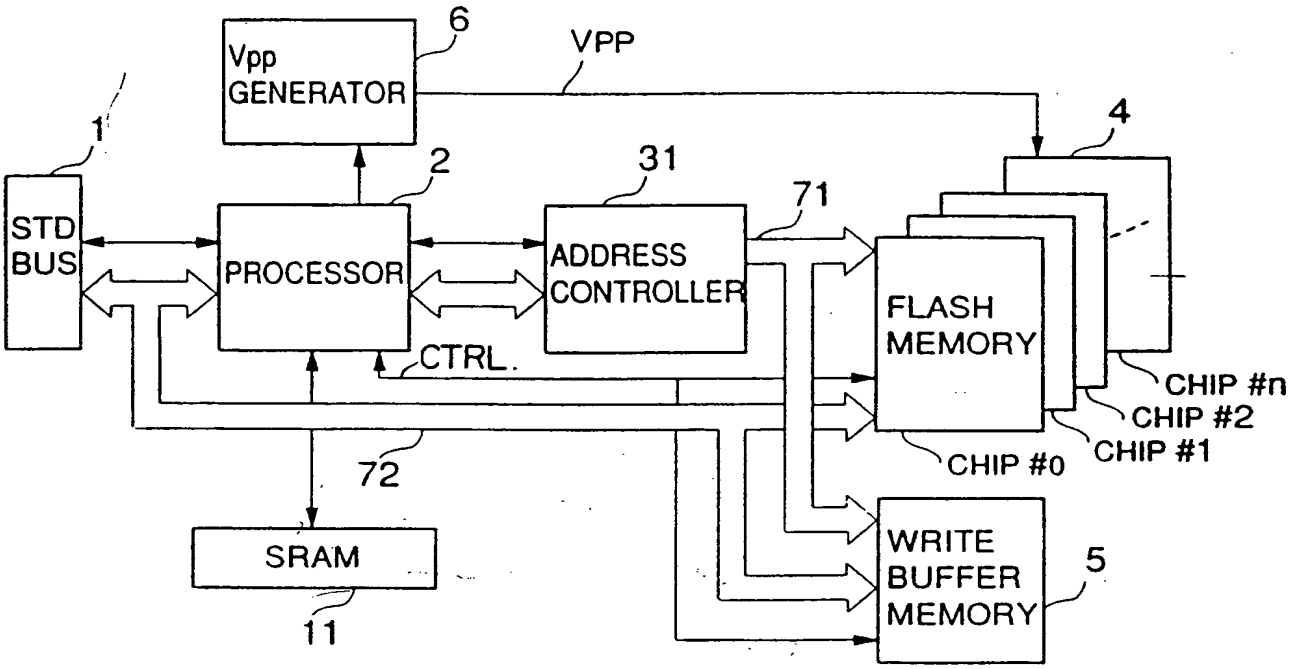

Vpp
GENERATOR
6
VPP
1
4
2
31
71
STD
BUS
PROCESSOR
ADDRESS
CONTROLLER
FLASH
MEMORY
CTRL.
CHIP #n
CHIP #2
CHIP #1
CHIP #0
72
SRAM
WRITE
BUFFER
MEMORY
5
11

FIG. 2

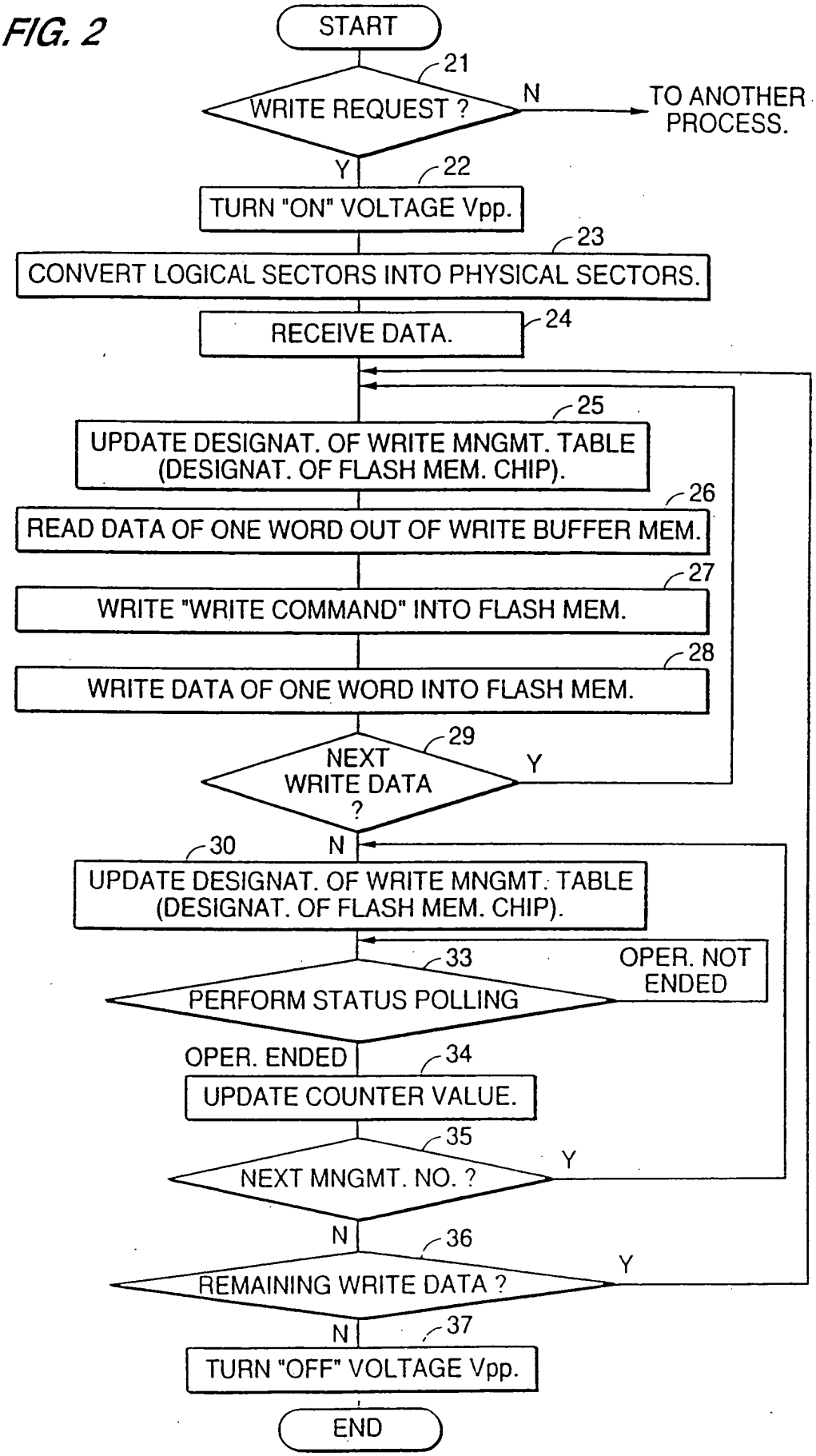

START
21
WRITE REQUEST ?
N
TO ANOTHER PROCESS.
Y
22
TURN "ON" VOLTAGE Vpp.
23
CONVERT LOGICAL SECTORS INTO PHYSICAL SECTORS.
24
RECEIVE DATA.
25
UPDATE DESIGNAT. OF WRITE MNGMT. TABLE (DESIGNAT. OF FLASH MEM. CHIP).
26
READ DATA OF ONE WORD OUT OF WRITE BUFFER MEM.
27
WRITE "WRITE COMMAND" INTO FLASH MEM.
28
WRITE DATA OF ONE WORD INTO FLASH MEM.
29
NEXT WRITE DATA ?
Y
N
30
UPDATE DESIGNAT. OF WRITE MNGMT. TABLE (DESIGNAT. OF FLASH MEM. CHIP).
33
PERFORM STATUS POLLING
OPER. NOT ENDED
OPER. ENDED
34
UPDATE COUNTER VALUE.
35
NEXT MNGMT. NO. ?
Y
N
36
REMAINING WRITE DATA ?
Y
N
37
TURN "OFF" VOLTAGE Vpp.
END

FIG. 3

MANAGE-MENT NO.	WRITE BUFFER MEMORY	FLASH MEMORIES (PHYSICAL SECTOR NOS.)		COUNTER
	BLOCK NO.	CHIP NO.	SECTOR NO.	
0	1	0	3	0
1	2	1	2	0
2	3	2	7	0
3	0	0	0	0
⋮	⋮	⋮	⋮	⋮

FIG. 4

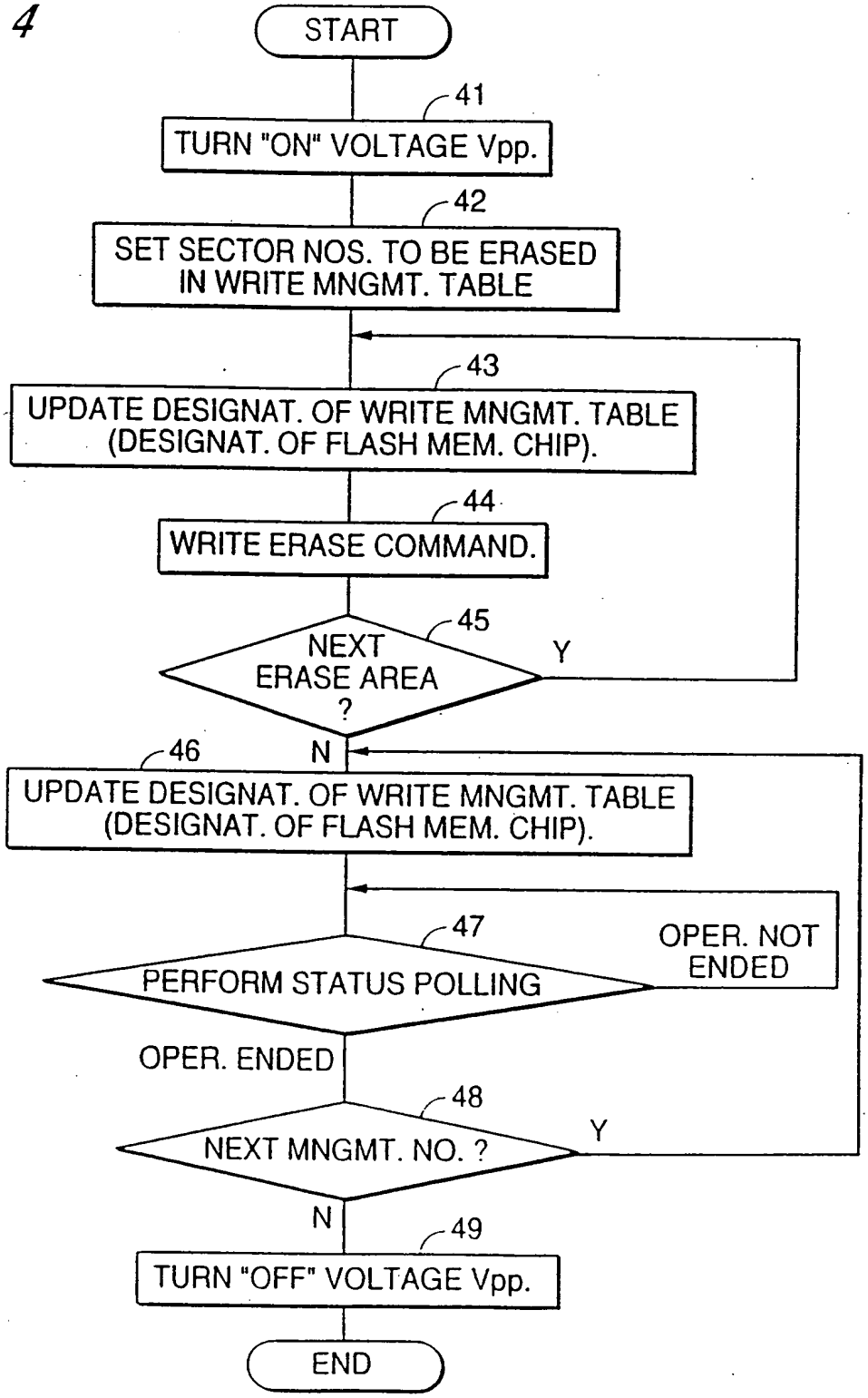

START
41
TURN "ON" VOLTAGE Vpp.
42
SET SECTOR NOS. TO BE ERASED IN WRITE MNGMT. TABLE
43
UPDATE DESIGNAT. OF WRITE MNGMT. TABLE (DESIGNAT. OF FLASH MEM. CHIP).
44
WRITE ERASE COMMAND.
45
NEXT ERASE AREA ?
Y
N
46
UPDATE DESIGNAT. OF WRITE MNGMT. TABLE (DESIGNAT. OF FLASH MEM. CHIP).
47
PERFORM STATUS POLLING
OPER. NOT ENDED
OPER. ENDED
48
NEXT MNGMT. NO. ?
Y
N
49
TURN "OFF" VOLTAGE Vpp.
END

FIG. 5

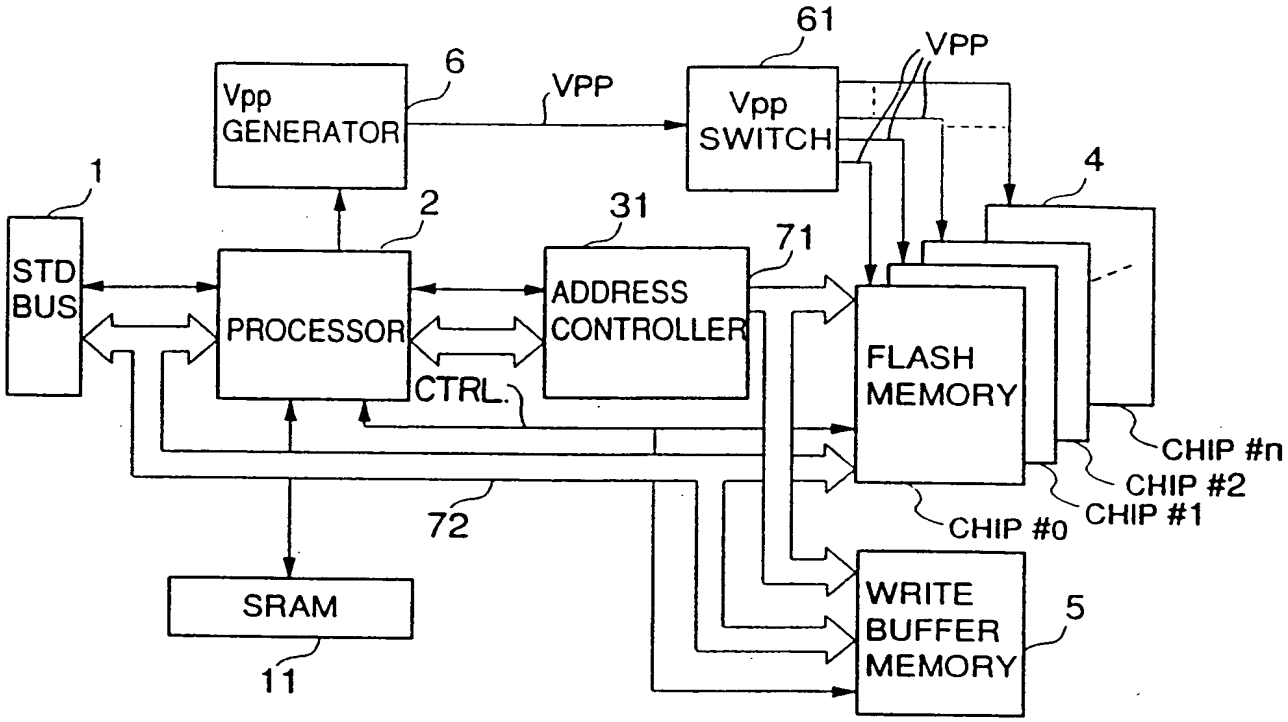

61
VPP
6
Vpp GENERATOR
VPP
Vpp SWITCH
4
1
2
31
71
STD BUS
PROCESSOR
ADDRESS CONTROLLER
FLASH MEMORY
CTRL.
CHIP #n
CHIP #2
CHIP #1
CHIP #0
72
SRAM
WRITE BUFFER MEMORY
5
11

FIG. 6

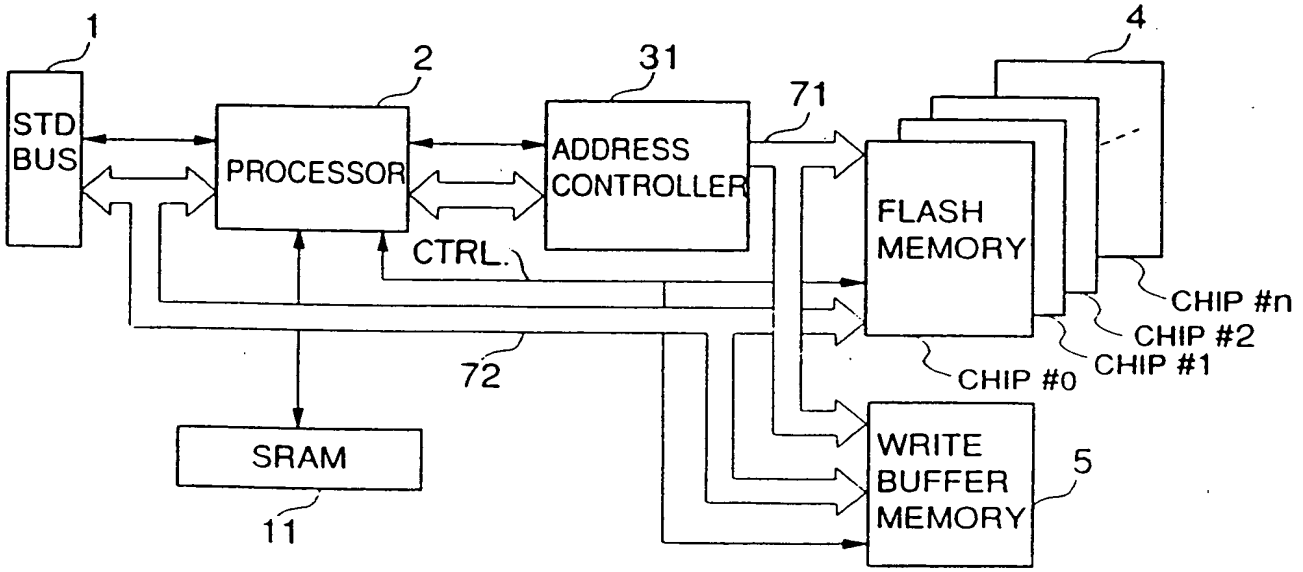
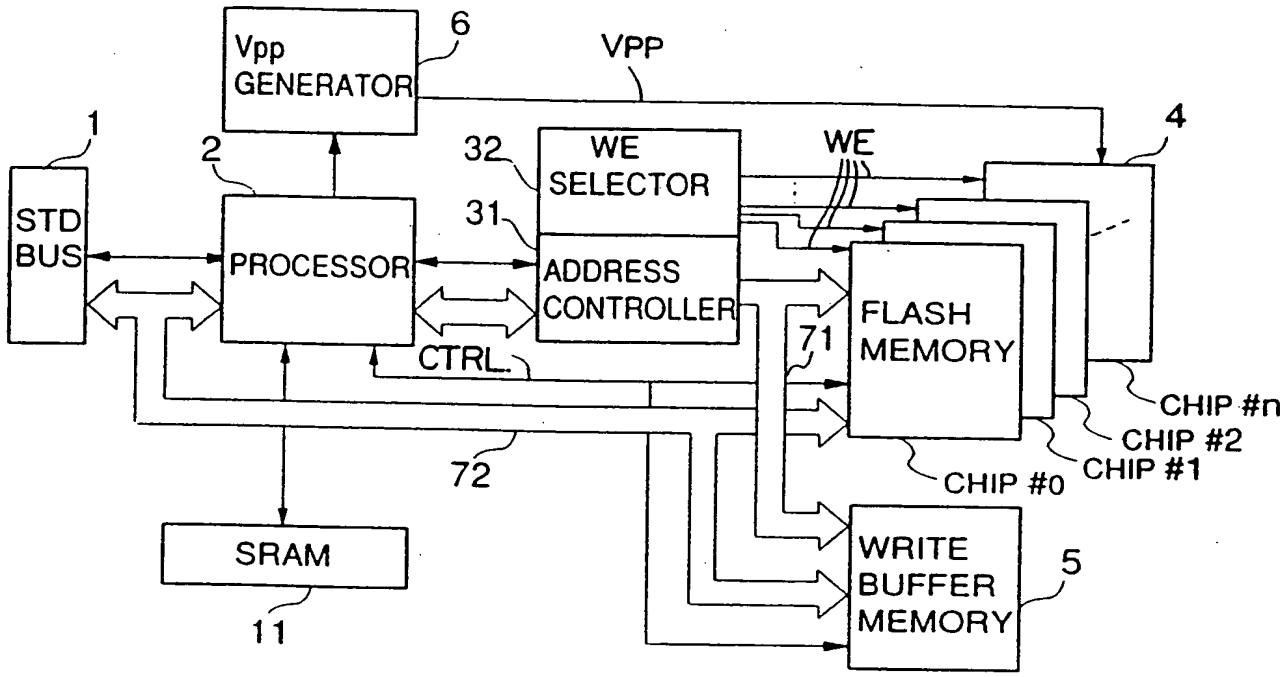

1
4
2
31
71
STD BUS
PROCESSOR
ADDRESS CONTROLLER
FLASH MEMORY
CTRL.
CHIP #n
CHIP #2
CHIP #1
CHIP #0
72
SRAM
WRITE BUFFER MEMORY
5
11

FIG. 7


Vpp GENERATOR
6
VPP
1
2
32
WE SELECTOR
WE
4
STD BUS
PROCESSOR
31
ADDRESS CONTROLLER
FLASH MEMORY
71
CTRL
CHIP #n
CHIP #2
CHIP #1
CHIP #0
72
SRAM
11
WRITE BUFFER MEMORY
5

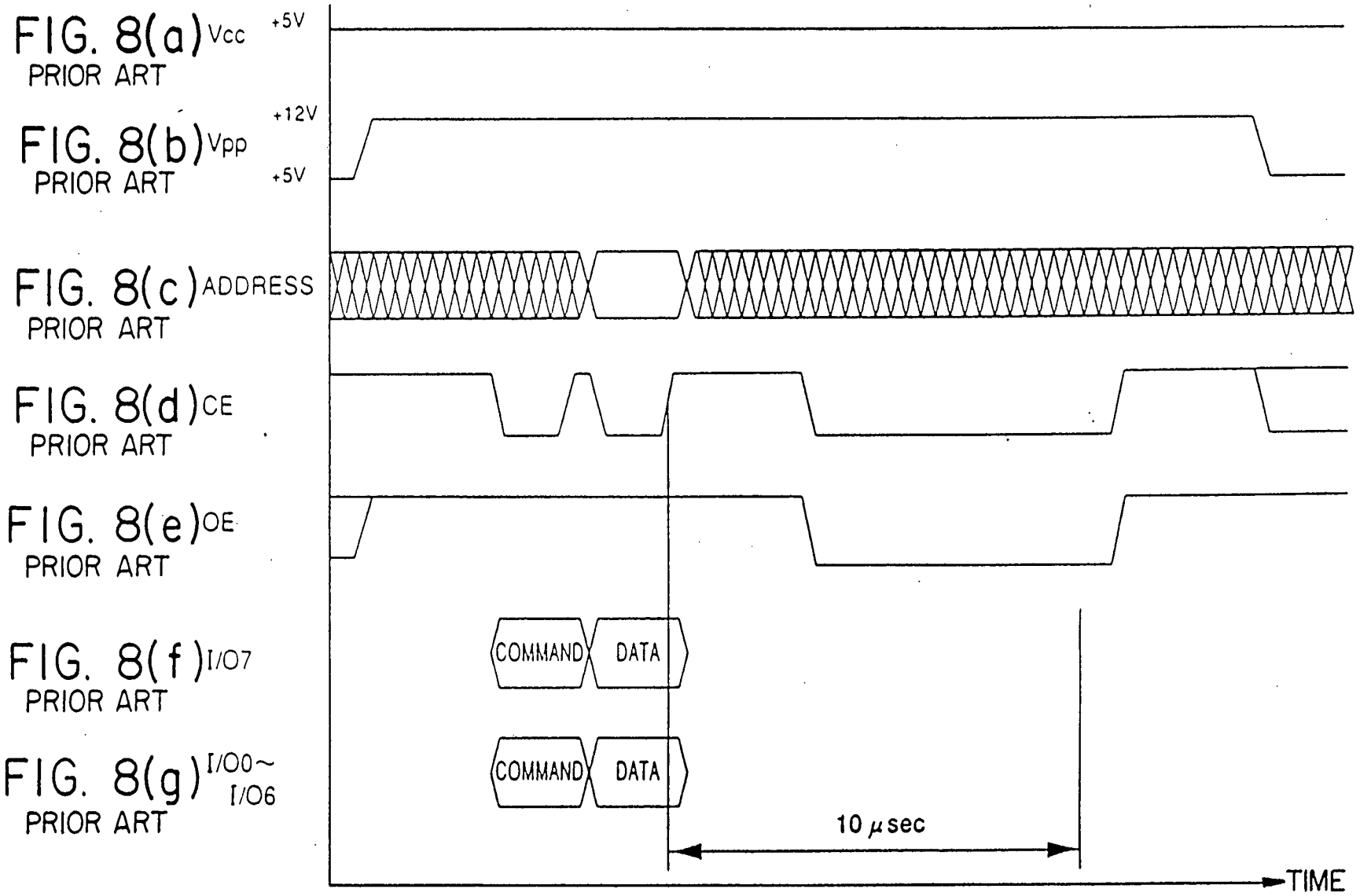
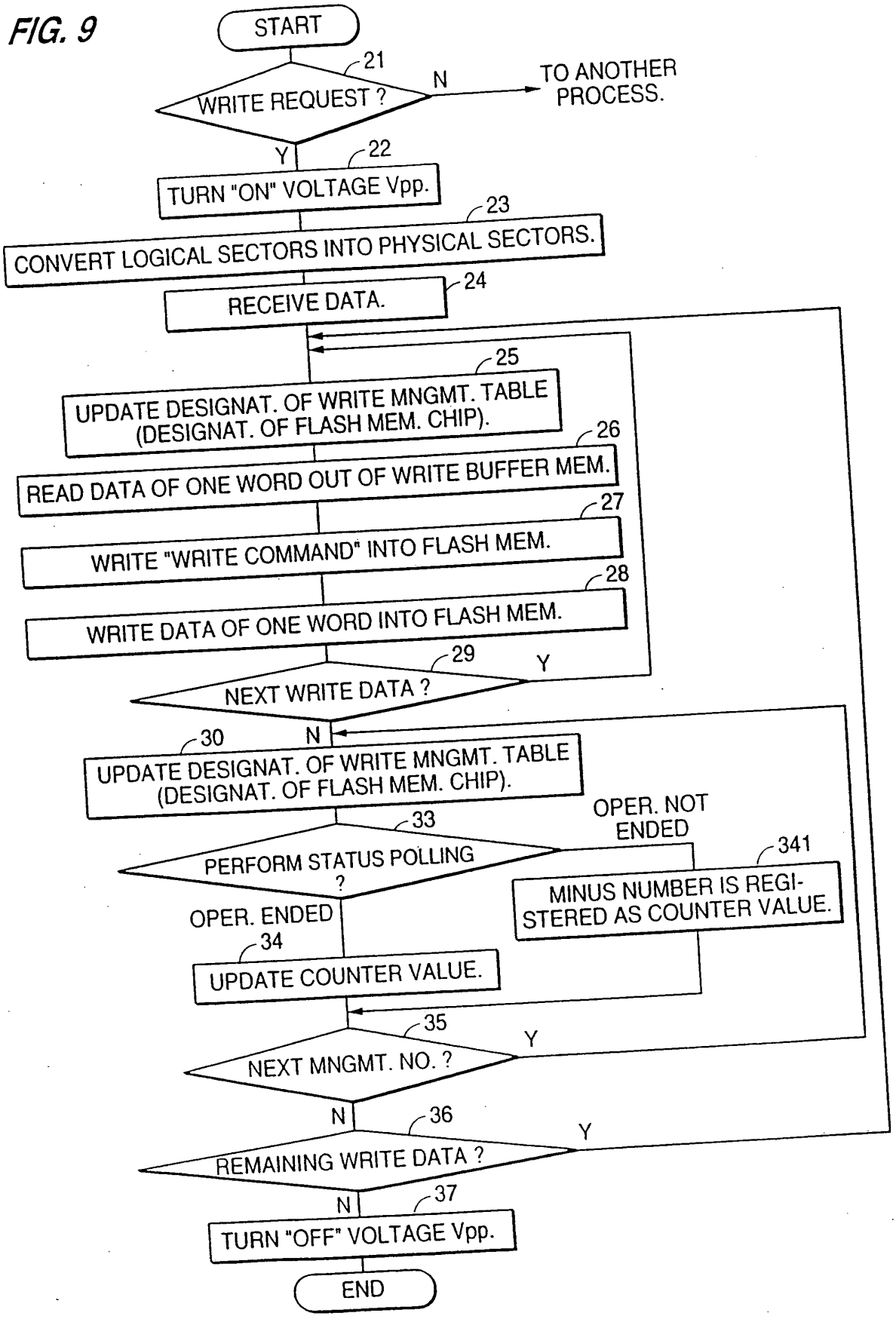


FIG. 8(a) Vcc
PRIOR ART
+5V
FIG. 8(b) Vpp
PRIOR ART
+12V
+5V
FIG. 8(c) ADDRESS
PRIOR ART
FIG. 8(d) CE
PRIOR ART
FIG. 8(e) OE
PRIOR ART
FIG. 8(f) I/O7
PRIOR ART
COMMAND
DATA
FIG. 8(g) I/O0~I/O6
PRIOR ART
COMMAND
DATA
10 μsec
TIME

FIG. 9


START
21
WRITE REQUEST ?
N
TO ANOTHER PROCESS.
Y
22
TURN "ON" VOLTAGE Vpp.
23
CONVERT LOGICAL SECTORS INTO PHYSICAL SECTORS.
24
RECEIVE DATA.
25
UPDATE DESIGNAT. OF WRITE MNGMT. TABLE (DESIGNAT. OF FLASH MEM. CHIP).
26
READ DATA OF ONE WORD OUT OF WRITE BUFFER MEM.
27
WRITE "WRITE COMMAND" INTO FLASH MEM.
28
WRITE DATA OF ONE WORD INTO FLASH MEM.
29
NEXT WRITE DATA ?
Y
N
30
UPDATE DESIGNAT. OF WRITE MNGMT. TABLE (DESIGNAT. OF FLASH MEM. CHIP).
33
PERFORM STATUS POLLING ?
OPER. NOT ENDED
341
MINUS NUMBER IS REGISTERED AS COUNTER VALUE.
OPER. ENDED
34
UPDATE COUNTER VALUE.
35
NEXT MNGMT. NO. ?
Y
N
36
REMAINING WRITE DATA ?
Y
N
37
TURN "OFF" VOLTAGE Vpp.
END